Design and Analysis of 32 Bit Regular and Improved Square Root Carry Select Adder

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***Abstract*— In modern VLSI technology transistors size is shrinking day by day for increasing speed and to reduce chip size, performance degradation is one of the major issues. As the technology scale down leakage power dissipation increases exponentially. In this paper a comparison among different parameters of square root carry select adders has been presented. These two 32 bit square root carry select adders are designed at 32nm technology. Performance of these sqrt carry select adders are evaluated and analysed in terms of delay, average power dissipation, power delay product and transistor count. Simulations are performed at 1.1v, with transistor length at 32nm. Their analysis reveals that improved 32 bit sqrt carry select adder has lesser delay, PDP as well as transistor count as compared to regular 32 bit sqrt carry select adder.**

***Keywords*— Square Root CSLA (SQRT CSLA), Binary to excess converter (BEC), RCA, ADDER, REGULAR.**

INTRODUCTION

Area power and delay reduction in data path logic systems are the main area of research in VLSI system design. High speed addition and multiplication has always been a basic requirement of high performance processors and systems. Addition is most normally and often used arithmetic operation on microprocessors, digital signal processors and especially on digital computers. Also it works as basic or fundamental building block for synthesis of all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structure becomes a critical hardware unit. In digital adders, the speed of addition is limited by time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The major speed limitation in any adder is in the production of carries and many authors have considered this problem[1]. The carry select adder is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum.

For the present work carry select adder has been selected because it has better speed as compared to other adders, also carry select adder is used in the square root style. In this work two 32 bit regular and improved square root carry select adders are implemented using transmission gate logic, then compared on the basis of transistor count, power, delay and PDP. Simulations are performed at 32nm technology with 1.1V power supply at 100MHz frequency. In the schematics all logic is designed using different gate width of NMOS and PMOS depending on their configuration whether they are connected in series or in parallel combination in a circuit and a minimum length of 32nm for NMOS and PMOS.

RELATED WORK

A. P. Thakarel and S. Agrawal's proposed work used very simple and efficient gate-level modification to reduce the area and delay of the CSLA. Based on this modification 8, 16-bit, and square-root CSLA architecture have been developed and it is compared with the regular SQRT CSLA architecture. The proposed design had reduced area as compared with the regular SQRT CSLA with reducing the delay [2].

Ch.Pavan Kumar R. Sravanthi and V. Narayana Reddy proposed work by using Binary to Excess-1 convertor for RCA with cin=1 to optimize the area and delay .This modified design will reduce area and power as compared with regular SQRT CSLA with only a slight increase in delay. Based on this modification 8, 16, 32, 64, 128-bit SQRT CSLA architecture and simulation will be developed and compare with regular SQRT CSLA [3].

Gajendra Kulshrestha proposed work uses a simple and an efficient gate-level modification using 45nm CMOS Process Technology, which drastically reduces the area and delay of the CSLA. Based on this modification 16-bit Carry Select Adder (CSLA) architectures have been developed and compared with the regular CSLA architecture developed in 180nm CMOS process technology. The proposed design has reduced area and delay to a great extent when compared with the previous CSLA developed in 180 nm. This work estimates the performance of the proposed designs with the regular designs in terms of delay, area and

power are implemented in Tanner (S-edit) tool. The results analysis shows that the proposed CSLA structure developed in 45 nm technology is better than the regular CSLA developed in 180nm technology [4].

A simple approach was proposed by B. Ram kumar and Harish M Kittur to reduce area and power of SQRT CSLA architecture. He had proposed design of 16 bit Low- Power and Area- Efficient Carry Select Adder. This work used a simple and efficient gate level modification to significantly reduce the area and power of the CSLA. Based on this modification 8, 16, 32 and 64 bit sqrt csla architecture have been developed and compared with the regular sqrt csla architecture.

The proposed design has reduced area and power as compared with the regular sqrt with only a slight increase in the delay. This work evaluates the performance of the proposed design in terms of delay, area, power and their products by hand with logical effort and through custom design and layout in 0.18 micrometer CMOS process technology.

The results analysis shows that the proposed CSLA structure is better than the regular sqrt csla [5].

PROPOSED WORK

A. CSLA

The linear carry-select adder is constructed by chaining a number of equal-length adder stages.

B. SQRT CSLA

The square root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage. It is also called as non-linear carry select adder. The SQRT CSLA is divided into m=√2m carry select stages (CSS), where m is number of input bits. The basic square root carry select adder has a dual ripple carry adder with 2:1 multiplexer.

1) Design of regular SQRT CSLA

The CSLA is used in many digital systems design to overcome the problem of carry propagation delay by independently performing addition operation by considering carry inputs (Cin) as 1 and 0.

Figure 1. shows a 32-bit SQRT CSLA. The 32 bit SQRT CSLA consists of 7 CSS. The CSS consists of two ripple carry adders one with carry in 0 and other with carry in 1. It also consists of a multiplexer which is used to select the sum and carry values from the two RCAs by using the control signal to it. The control signal to multiplexer is nothing but the carry out of the previous CSS. If the control signal is 1 then sum and carry out of RCA with Cin=1 is selected by the multiplexer and if control signal is 0 then sum and carry out of RCA with Cin=0 is selected by the multiplexer.

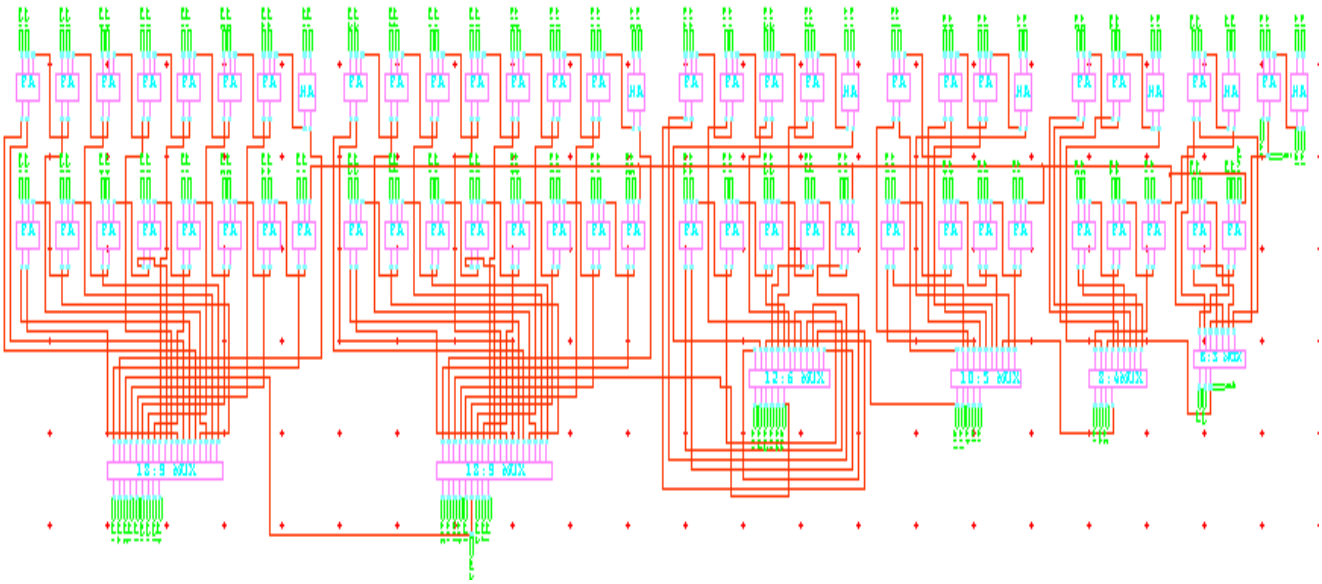

Fig.1. 32 bit regular SQRT CSLA

In above 32 bit SQRT CSLA design, full adder and half adders are designed using transmission gate logic.

2) Design of improved SQRT CSLA

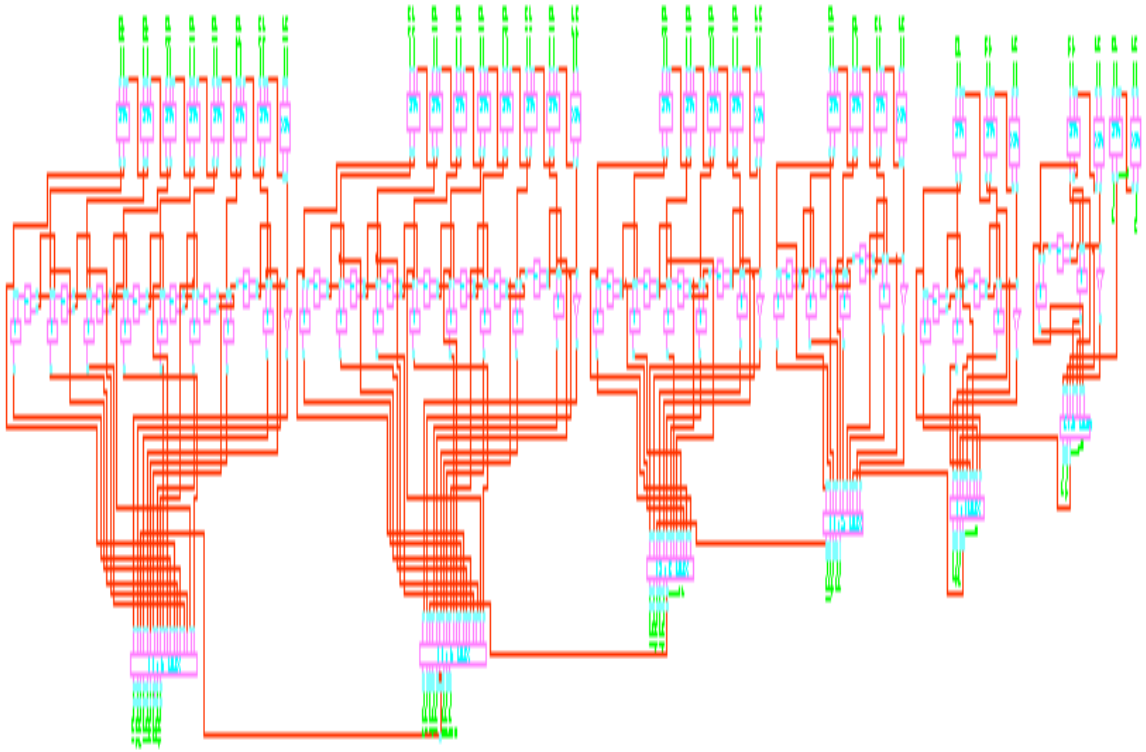

Fig. 2. 32 bit improved SQRT CSLA

SIMULATED WAVEFORMS

A. WAVEFORMS OF REGULAR SQUARE ROOT CARRY SELECT ADDER

In regular 32 bit square root carry select adder, when Cin is equal to 1 in 2nd chain of ripple carry adders, we add Cin is equal to 1 in starting of 2nd chain of ripple carry adders of each stage of regular sqrt csla. The Simulation waveforms of regular square root carry select adder are shown in Figure 3, 4 and 5.

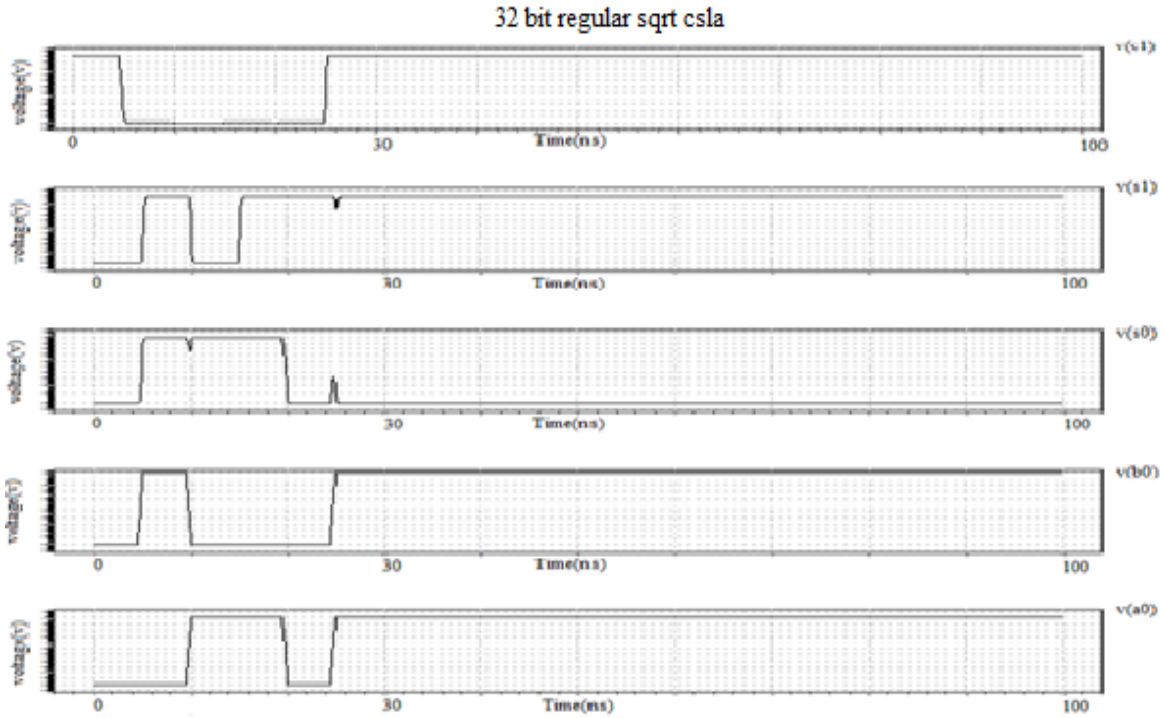

Fig. 3. Output waveform of 1st stage of 32 bit regular square root carry select adder

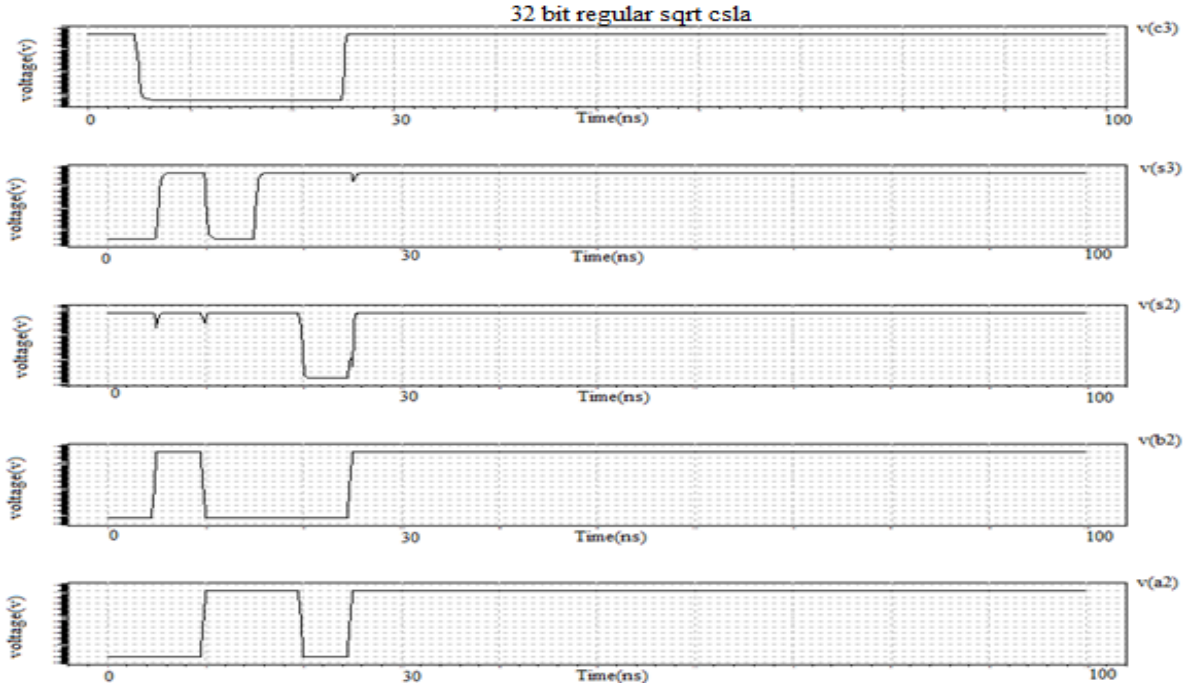

Fig. 4. Output waveform of 2nd stage of 32 bit regular square root carry select adder

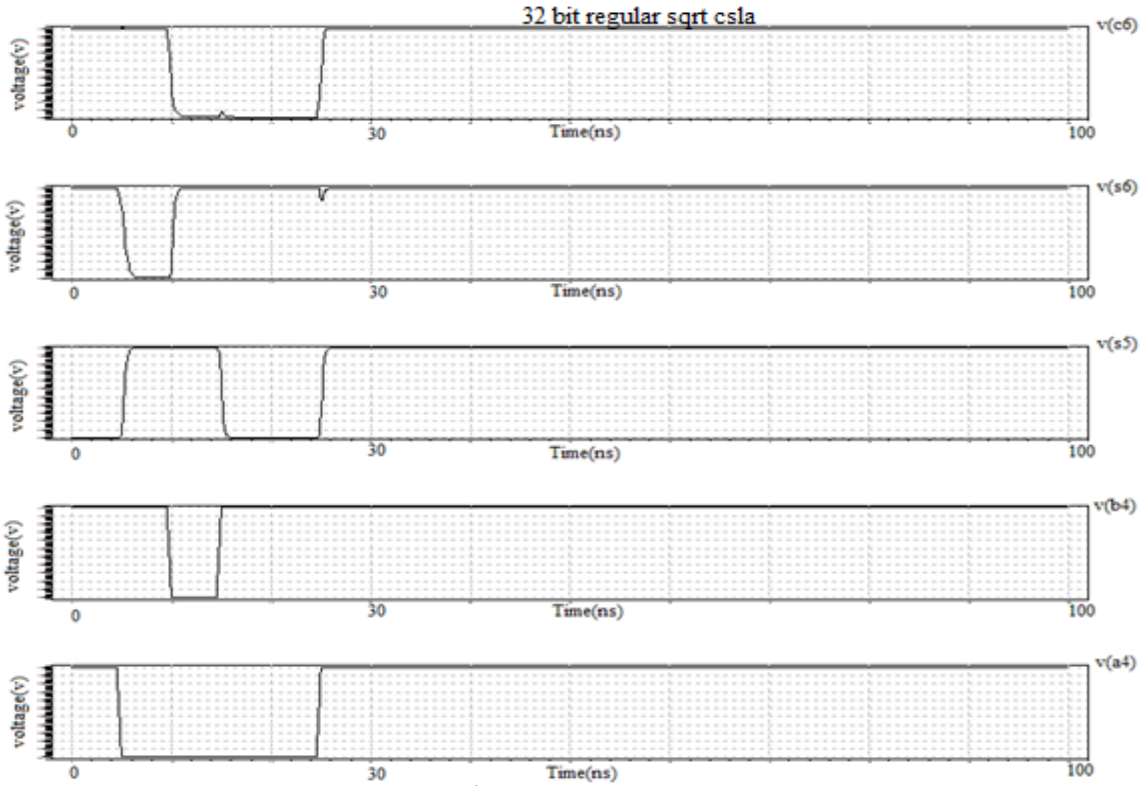

Fig. 5. Output waveform of 3rd stage of 32 bit regular square root carry select adder

Similarly for next stages we can simulate the circuit and can achieve waveforms.

B. Waveforms of improved square root carry select adder

In improved 32 bit square root carry select adder, instead of ripple carry adders we use binary to excess converter (BEC) in 2nd chain of sqrt csla. In this, BEC is used for increasing the each output bit by 1, so there is no need of adding Cin is equal to 1 in inputs, because adding Cin is equal to 1 has also same purpose to increase each output bit by 1.The Simulation waveforms of regular square root carry select adder are shown in Figure 6 and 7.

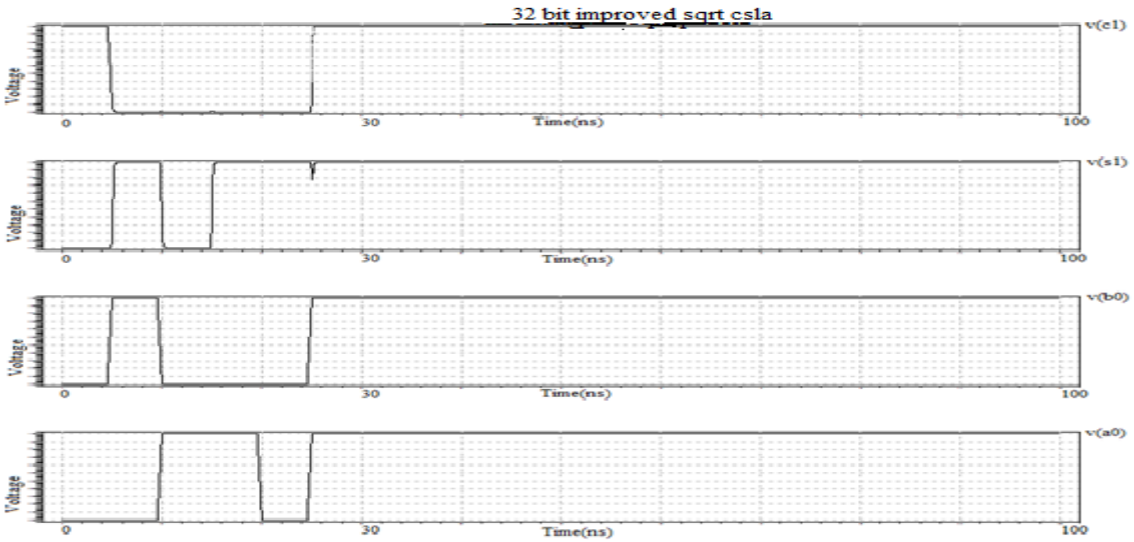

Fig. 6. Output Waveform of 1st Stage of 32 Bit Improved square Root Carry Select Adder

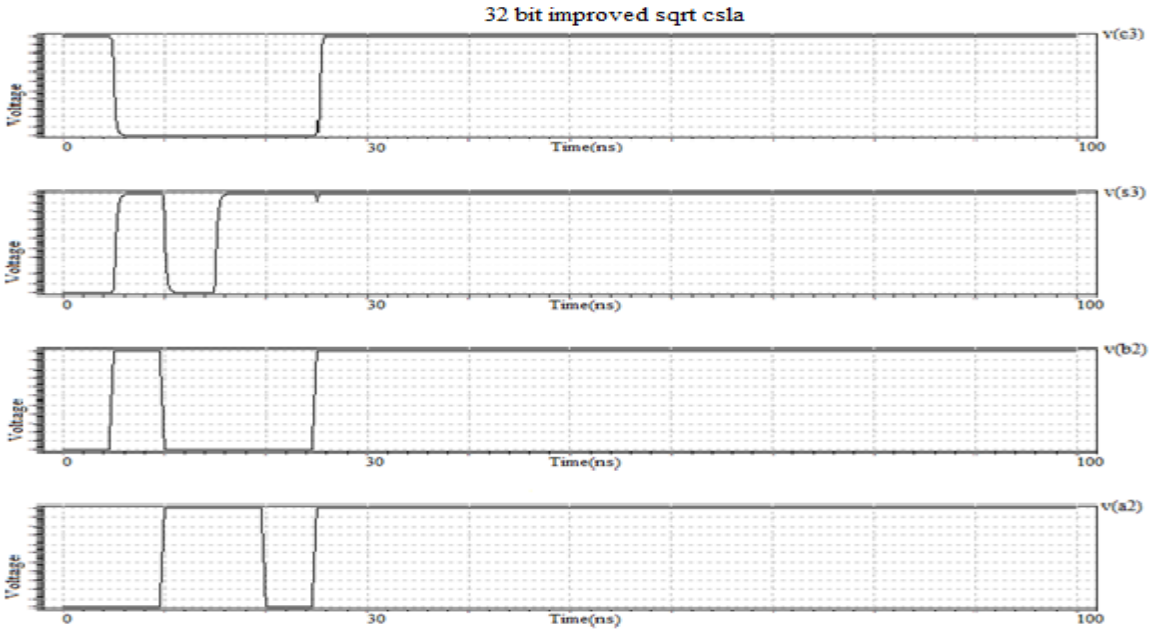

Fig. 7. Output Waveform of 2nd Stage of 32 Bit Improved square Root Carry Select Adder

RESULTS

In the following tables, comparison of performance parameters such as power, delay, transistor count and power delay product of 32 bit regular square root carry select adder and 32 bit Improved sqrt carry select adder is shown below.

A. Power and delay comparison of square root carry select adders

In the present work we have compared the parameters power and delay of regular sqrt csla and Improved sqrt csla. Comparison of power and delay are shown in the Table 1 and Figure 8 .

Table 1: Comparison of power and delay

Square root Carry Select Adder	Power (µw)	Delay(ns)
Regular	55.89	3.40
Improved	63.17	1.97

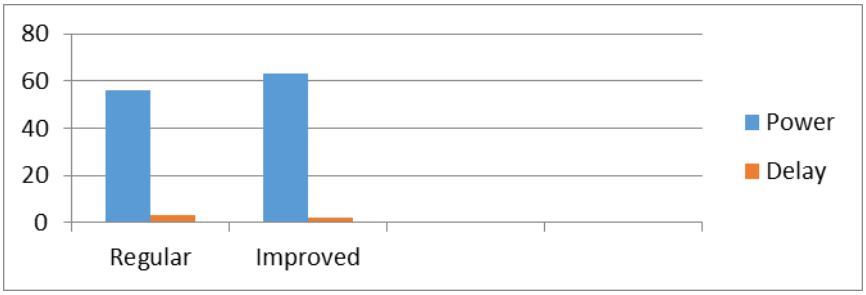

Fig. 8. Power and Delay comparison of square root carry select adders

B. Transistor count and PDP comparison of square root carry select adders

In the present work we have compared the parameters transistor count and PDP of regular sqrt csla and improved sqrt csla. Comparison of transistor count and PDP are shown in the Table 2 and Figure 9.

Table 2: Comparison of transistor count and PDP

Square root Carry Select Adder	Transistor Count	PDP (fj)
Regular	1414	190.026
Improved	1390	124.445

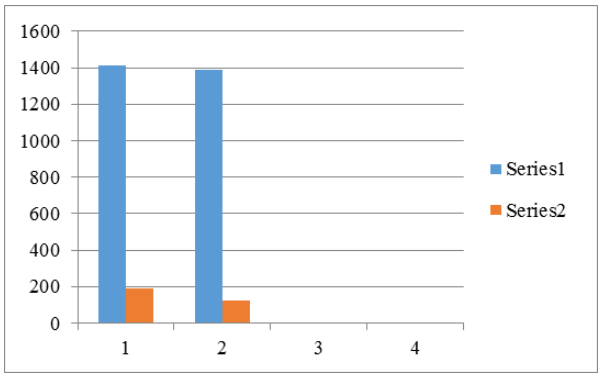

Fig. 9. Transistor Count and PDP comparison of square root carry select adders

C. Comparison of Power, delay and PDP of square root carry select adders

In this present work we have compared the parameters power, delay and PDP of regular sqrt csla and improved sqrt csla. Comparison of power, delay and PDP are shown in the Table 3 and Figure 10.

Table 3: Comparison of power, delay and PDP

Square root Carry Select Adder	Power (µw)	Delay(ns)	PDP(fJ)
Regular	55.89	3.40	190.026
Improved	63.17	1.97	124.445

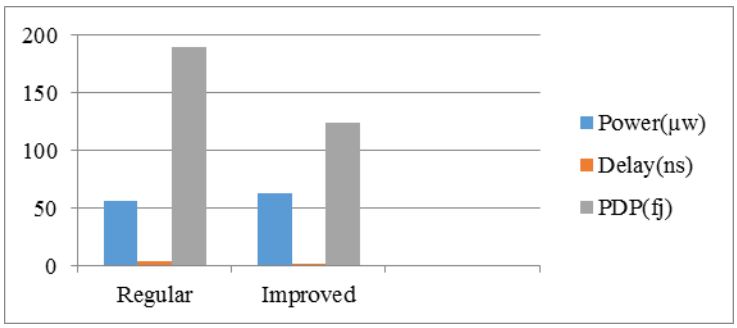

Fig. 10. Power, Delay and PDP comparison of square root carry select adders

CONCLUSIONS

A 32 bit regular square root carry select adder and 32 bit improved square root carry select adder is designed architecture in this paper. Simulation results have been carried out using T-Spice at 32nm technology. All the simulations of improved 32 bit square root carry select adder are carried out with 1.1v at 100MHz frequency. Results show that improved 32 bit square root carry select adder has power dissipation is 63.17mw, delay is 0.26ns and PDP is 124.445fj, and all the performance parameters shows improvement as compared to the 32 bit regular square root carry select adder.

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